Commissioner=s Decision #1282

Décision du Commissaire #1282

TOPIC: F01, G00, 000,

SUJECT: F01, G00, O00

Application No : 2,338,458

Demand no : 2,338,458

COMMISSIONER'S DECISION SUMMARY

C.D.1282, Application 2,338,458

Anticipation, Obviousness, Inoperative

The Examiner rejected this application for being anticipated by public disclosure of the claimed subject matter before the claim date. The Examiner also alleged that the subject matter of the claims is obvious and alleged that one of the claims is inoperative.

The application was refused.

IN THE CANADIAN PATENT OFFICE

DECISION OF THE COMMISSIONER OF PATENTS

Patent application number 2,338,458 having been rejected under Subsection 30(3) of the *Patent Rules*, the Applicant asked that the Final Action of the Examiner be reviewed. The rejection has been considered by the Patent Appeal Board and by the Commissioner of Patents. The findings of the Board and the decision of the Commissioner are as follows:

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INTRODUCTION

1. This decision deals with a request that the Commissioner of Patents review the Examiner's Final Action rejecting patent application number 2,338,458 which was filed on February 27, 2001 and is entitled AMETHOD AND VLSI CIRCUITS ALLOWING TO CHANGE DYNAMICALLY THE LOGICAL BEHAVIOUR@. The Applicant and Inventor is Mr. Ioan Dancea, who represented himself in correspondence with the office. The Examiner in charge issued a Final Action on December 23, 2003 objecting to claims 1 to 12 based on lack of novelty, obviousness and insufficient elements for proper operation.

2. At the Applicant=s request, the Patent Appeal Board conducted a hearing via teleconference on April 5, 2005, at which time the inventor, Mr. Ioan Dancea, represented himself. The Patent Office was represented by Mr. Andrew O=Malley and his Section Head, Mr. Peter Ebsen.

3. Mr John Cavar was a member of the Board at the hearing but he has retired from the Public Service and did not take part in the preparation of this recommendation to the Commissioner.

BACKGROUND

4. The invention involves a product terms method that permits dynamically changing the logical behaviour of combinational or synchronous sequential circuits. The method makes use of three Amemory words@, namely: mask word, product word, and function word which describe the relationship between the input variables and the Boolean output functions that describe the logical behaviour. The application also provides a hardware structure for several types of VLSI circuits, which have reconfigurable logic behaviours using the three memory words. An expert system which can be used to generate the tables of memory words and configure the VLSI circuits implementing the product terms method is also included.

5. This application has 12 claims on file, submitted on June 16, 2003 in response to the Examiner=s report dated January 27, 2003.

6. Claim 1 sets forth a method for reconfiguring a VLSI device, and is as follows:

> 1 A computer assisted method for changing the logical behaviour of a dynamically re-configurable VLSI device from one target circuit to other target circuit, comprising an interface which allows to receive a configuration or reconfiguration request, a peripheral adapter for managing the configuration processes and an expert system, and further comprising the steps of:

(a) receiving a configuration or re-configuration request from a user or a running program to configure or to re-configure the said VLSI device to a target circuit defined by one or several groups of sum-of-product logical equations; and

(b) configuring or re-configuring the said VLSI device by the said expert system to processes the sum-of -product logical equations.

7. Claims 2 to 7 pertain to the particular VLSI device which can be used in the method in order to be reconfigurable into different circuits. Claims 2 and 3 are as follows:

2 A dynamically re-configurable VLSI device as recited in claim 1 for implementing combinational circuits defined by a group of sum-of-products logical equations, comprising:

"m" input terminals connected to an input register for storing the input variables;

"n" cells, a cell C(k) for determining a logical value of a product term p(k)of said logical equations corresponding to said input variables, where "k" is an integer k [1 ,n]; and

a block of "r" OR gates, each gate having "n" inputs, connected to said cells C(k) for receiving said logical value of said product terms p(k) and providing a logical value for each said logical equations at Ar" output terminals.

3 A dynamically re-configurable VSLI[sic] device as defined in claim 2, wherein said cell C(k) comprises:

a registers storage area for storing a mask word, a product word and a function word, representative of said product term p(k);

first logic level means for receiving said "m" input variables and logical values of said mask word to generate intermediate results;

second logic level means for comparing said logical values of said product word with said intermediate results to determine said logical value of said product term p(k); and

third logic level means for transferring said function word to said "r" output terminals, according to said logical value of said product term p(k).

8. The remaining device claims 8 to 11 set forth other embodiments for a reconfigurable VLSI device, and claim 12 pertains to a method claim which recites elements of an expert system for use with the method of claim 1.

ISSUES

The Final Action presents the following questions to the Board:

1. Are claims 1 to 12 anticipated under Subsection 28.2(1)(a) of the *Patent Act*?

2. Are claims 1 to 12 obvious under Section 28.3 of the *Patent Act*?

3. Is claim 12 inoperable under Section 2 of the *Patent Act*?

REFERENCES APPLIED

Dancea[1]: Dynamically Changing the Logical Behaviour of a Microcomputer Interface; IEEE Micro; Volume 9 Number 2; April 1989; pages 39 to 51;

Dancea[2]: A Software Method for Implementation of Digital Circuits in Microcomputer Systems; Proceedings of the ISMM International Symposium; Beverly Hills, California; February 5 to 7,

1986; pages 145 to 148; and,

Dancea[3]; An Expert System to Generate and/or Modify the Logical Behaviour of a Microcomputer Interface; Proceedings of the ISMM International Symposium; Honolulu, Hawaii; February 1 to 3, 1988; pages 148 to 152.

ANTICIPATION

The Examiner's position

9. In the Final action, the Examiner objected to claims 1 to 12 under Section 28.2(1)(a), as being disclosed by the Applicant more than 1 year before the filing date of this application, stating in part:

> Figure 6 of Dancea[1] shows an expert system connected to a hardware driver and a simulated structure. The expert system interacts with a user to initiate a configuration process (Dancea[1], page 43, column 1, lines 30 to 45); the first decision box of figure 3 (Dancea[1], figure 3, line 1) illustrates this interaction. The expert system subsequently configures the driver and the simulated structure (Dancea[1], page 46, column 2, lines 26 to 28); the last action box of figure 3(Dancea[1], figure 3, line 6) illustrates this step. Dancea[1] states that the method can be implemented by a VLSI circuit (Dancea[1], page 50, column 2, lines 1 to 12). Claim 1 is [sic] therefore lacks novelty in view of Dancea[1].
>
> Dependent method claim 12 defines the method of claim 1 by structure only. Thus, claim 12 does not distinguish over claim 1, since there are no further patentable method steps defined.

Device claim 2, although dependent on method claim 1, defines some structure of the VLSI circuit, namely input terminals, cells, and OR gates. As illustrated by figure 12 of Dancea[1], input terminals are shown at the top of the figure, the basic cell is shaded in grey, and the OR gates are shown in the bottom left-hand comer. Claim 2 thereby lacks novelty in view of Dancea[1].

Dependent apparatus claims 3 to 12 recite further details of the internal arrangements of the cell and various input/output conditions to be used with the cell, per below. There are no novel features to be found, and claims 3 to 12 also lack novelty.

A configurable VLSI device for implementing logical behaviours defined by a group of "sum-of-product" equations employing a series of basic cells with storage space for "mask," "product,"and ''function'' words and the necessary logic for determining "product terms" as recited in. claims 2 to 7 has been disclosed in Dancea[1] (page 50, column 2, lines 1 to 12). Particular reference is paid to figure 12, which shows registers and logic blocks for performing the functions recited by claims 2 through 7.

Claims 8 and 9 recite the implementation of a single-output combinational circuit via the VLSI device of claim 1. Dancea[2], which is similarly directed at the same circuit simulating method employed by Dancea[1] and the current application, discloses the use of the sum-of-products method for single output combination circuits (Dancea[2], page 145, column 2, lines 1 to 41). Claims 8 and 9 thereby lack novelty in view of Dancea[1] and Dancea[2].

Similarly, claims 10 and 11 are disclosed in Dancea[1] and Dancea[2]; particularly with reference to the discussion of multiple-output and synchronous sequential circuits in Dancea[2] (page 145, column 2, line 43 to page 146, column 1, line

55).

Regarding claim 12, an expert system used to define the logical behaviour of digital circuits expressed as "sum-of-product@ equations is disclosed by Dancea[1]. Figure 3 shows the operation of the expert system, and figure 4 shows in greater detail the operations taken by the expert system to process the sum-of-product equations of the target circuit (line 4 of figure 3). The steps illustrated by figures 3 and 4 of Dancea[1] correspond to the means recited by claim 12. Claim 12 thereby lacks novelty in view of Dancea[1].

The Applicant's response

10. In response to the Final action, the Applicant in a letter dated February 27, 2004 requested a hearing and said that he had already given detailed responses to the same arguments in his previous correspondence with the office.

11. In his letter dated October 21, 2002 the Applicant had this to say about the prior Dancea[1] publication.

Obviously, the predicted possible hardware solution (Figure 12 and the attached description from the mentioned publication) has common elements with the solution presented in the claims 5 to 10 of the patent application, because the second represents the evolution of the first, but the two solutions are different. Considering only an example, precisely the use of one of the simplest hypothetic re-configurable VLSI circuit, as described by claims 5 to 10, which can materialize, among others, the target circuit defined by equations (1) (page 8) of patent application. These equations have 5 product terms. Between these product terms, the term aANDb is present in all three equations. Consequently,

the basic cell of Figure 12, publication Dancea[1], must have in the block "OR ports" at least three OR gates. As it is known, in a complex structure all basic cells having a determined function must have the same architecture. So, the 5 product terms of the proposed structure need 15 OR gates, number larger superior to the real 3 OR gates necessary by the implementation described in the patent application. In reality, with standard outputs for every basic cell, saying 8 or 16 outputs, and with several hundreds of product terms, the excess of OR gates, and the presence of the comparator in Dancea[1] publication instead of XNOR gates, multiply by several orders the number of gates found in the architecture of the proposed VLSI circuit of the patent application.

12. On page 2 of his letter dated October 21, 2002, the Applicant pointed out the unique aspects of the VLSI circuits described in his application:

To apply this special mode of synthesis the applicant made use of a technique of Boolean algebra, named *perfect induction* (it is not a classical synthesis method). A proof by perfect induction involves substituting all possible combinations of values for the logical variables in the two implementations (one solution which implements directly the target circuit and the second solution which implements the target circuit using the circuit for circuits), and verifying that the two solutions give the same result for all possible combinations (for more detail refer to chapter 2 of "Logic Design Principles" by Edward J. McCluskey, Prentice Hall, 1986).

. . .

No skilled person in the art of digital design can arrive at the proposed VLSI circuits via a classical synthesis, because any classical synthesis need to know the inputs, the outputs, the number and the succession of states. Since all of the VLSI circuits proposed in the application are of type circuit for circuits, which can implement many different target circuits, the skilled person in the art of digital

design do not know any of these parameters. Consequently, it must use other modes of synthesis, as the applicant explained the technique of perfect induction. What the applicant wanted to mention in the previous correspondence is the fact that a skilled person in the art of digital design, normally finds himself in the situation to develop a completely specified functional circuit, similar to a so called target circuit in the present application, for which the inputs, the outputs, the number and the succession of states are known. Thus, to implement this completely specified functional circuit, he/she will use one of the classical synthesis methods, learned at school or found in references. These statements are completely different from the examiner's affirmation.

Legal Principles - Anticipation

13. Subsection 28.2(1) of the *Patent Act* provides, in part:

> Subject-matter of claim must not be previously disclosed
>
> 28.2 (1) The subject-matter defined by a claim in an application for a patent in Canada (the "pending application") must not have been disclosed
>
> (a) more than one year before the filing date by the applicant, or by a person who obtained knowledge, directly or indirectly, from the applicant, in such a manner that the subject-matter became available to the public in Canada or elsewhere;
>
> (b) before the claim date by a person not mentioned in paragraph (a) in such a manner that the subject-matter became available to the public in Canada or elsewhere;

14. To address anticipation by prior publication, we are guided by the test described by Justice Hughes in *Janssen-Ortho Inc. v. Novopharm Ltd.*, [2006] F.C.J. No. 1535, 2006 FC 1234, where he applied the Supreme Court of Canada decision in *Free World Trust v. Électro Santé Inc.* (2000), 9 C.P.R. (4th) 168 (S.C.C.) [*Free World Trust*] as follows:

> 105 The Supreme Court of Canada in *Free World Trust v. Électro Santé Inc.*, [2000] 2 S.C.R. 1024, 2000 SCC 66 outlined the test for anticipation is [sic] in Canada. The Court said at paragraph 26:
>
> > ... The legal question is whether the Solov'eva article contains sufficient information to enable a person of ordinary skill and knowledge in the field to understand, without access to the two patents, "the nature of the invention and carry it into practical use without the aid of inventive genius but purely by mechanical skill" ... In other words, was the information given by Solov'eva for [the] purpose of practical utility, equal to that given in the patents in suit"?: ... as was memorably put in *General Tire & Rubber Co. v. Firestone Tyre & Rubber Co.*, [1972] R.P.C. 457 (C.A.) at p. 486:
> >
> > A signpost, however clear, upon the road to the patentee's invention will not suffice. The prior inventor must be clearly shown to have planted his flag at the precise destination before the patentee.
>
> The test for anticipation is difficult to meet:
>
> > One must, in effect, be able to look at a prior, single publication and find in it all the information which, for practical purposes, is needed to produce the claimed invention without the exercise of

> any inventive skill. The prior publication must contain so clear a direction that a skilled person reading and following it would in every case and without possibility of error be led to the claimed invention. [*Beloit Canada Ltd. v. Valmet OY* (1986), 8 C.P.R. (3d) 289 (F.C.A.), per Hugessen J.A., at p. 297].

> 106 The House of Lords in *Synthon v. SmithKline Beecham PLC's Patent*, [2005] UKHL 59 para. 19 (Lexis), [2006] 1 All. E.R. 685, [2006] RPC 10 has put the matter succinctly: there are two requirements for anticipation, enablement and disclosure.

15. Before considering validity, the claims must be purposively construed. Construction will reveal that some elements thereof are essential, while others are non-essential (*Free World Trust*, *supra*; *Whirlpool Corp. v. Camco Inc.*, [2000] 2 S.C.R. 1067, 9 C.P.R. (4th) 129). The claims, as purposively construed, are the focus in determining anticipation. In order to satisfy the above-stated *Beloit* test, a single, prior publication must disclose all of the essential elements of a claim. In Free World Trust, at para 25, the Supreme Court stated [emphasis added]:

> Anticipation by publication is a difficult defence to establish because courts recognize that it is all too easy after an invention has been disclosed to find its antecedents in bits and pieces of earlier learning. It takes little ingenuity to assemble a dossier of prior art with the benefit of 20-20 hindsight. In this case, the respondents contended that all of the essential elements of the appellant's alleged inventions were disclosed in a single publication, the Solov'eva article, which predated the patent application by almost 4 years. If this is correct, the patent would be invalid.

16. In *Dimplex v. CFM*, 2006 FC 586, after the Court construed the claims according to

the principles set forth by the Supreme Court in *Whirlpool* and *Free World Trust* (see paras 49-52 of *Dimplex*), in considering the question of anticipation, the Court applied the *Beloit* test. The Court went on to consider the question of anticipation and stated at para 105 that only the essential elements of the claims were to be considered in comparing the claims with the prior art [emphasis added]:

> ...As discussed above, I am satisfied that Butterfield did not disclose all of the essential elements of the disputed claims, notably the flicker element and flame effect element. One could not find in Butterfield all the information needed to produce the claimed invention without the exercise of additional inventive skill.

17. With respect to anticipation, it has long been a requirement in Canadian law that only the material, or essential elements, of the claims be disclosed in the prior art. Hughes J. *et al.* In *Hughes and Woodley on Patents* (2008), at '10, page 134, citing *Brushtech Inc. v. Liberty Home Products Corp.*, [1988] 21 C.I.P.R. 27, 23 F.T.R. 300, 23 C.P.R. (3d) 370 state:

> However, where the document would clearly show the same invention, apart from an element readily understood, there is anticipation.

18. In *Xerox of Canada Ltd. v. IBM Canada Ltd.* 1977 CarswellNat 669, 33 C.P.R. (2d) 24 Collier, J. stated:

> 68 Thorson, P., summarized the precedents in *The King v. Uhlemann Optical Co.* (1949), 11 C.P.R. 26 at pp. 41-3, [1950] Ex. C.R. 142, 10 Fox Pat. C. 24 at pp. 38-40; affirmed 15 C.P.R. 99 at p. 104, [1952] 1 S.C.R. 143 at p. 151, 12 Fox Pat. C. 65:
>
> > I now come to the attacks on the patent. Lack of novelty and lack of subject-matter as grounds for holding a patent invalid are closely related, but are not the same. Lindley L.J. pointed out the difference in *Gadd & Mason v. Mayor, etc. of Manchester* (1892), 9 R.P.C. 516 at pp. 525-6: "In considering subject-matter, novelty is assumed; the question is whether, assuming the invention to be new, it is one for which a patent can be granted. In considering novelty, the invention is

> assumed to be one for which a patent can be granted if new, and the question is whether on that assumption it is new. Has it been disclosed before? If there is an earlier specification for the very same thing, the second invention is not new; but if the two things are different, the nature and extent of the difference have to be considered. The question then becomes one of degrees. But, unless it can be said that the differences are practically immaterial; that there is no ingenuity in the second invention, no experiment necessary to show whether it can be usefully carried out or not, the second cannot be said to have been anticipated by the first."

19. Similarly, in *Cabot Corp v. 318602 Ontario Ltd.,* 1988 CarswellNat 569, 19 C.I.P.R. 204, 17 F.T.R. 54, 20 C.P.R. (3d) 132 at paragraph 46 Rouleau J., stated:

> As Mr. Fox quoted, referring to a patent which was attacked for lack of novelty, in his notable text *Canadian Law and Practice Relating to Letters Patent for Inventions* , 4th ed. (Toronto: Carswell, 1969) at 101-102:
>
> > Has it been disclosed before? If there is an earlier specification for the very same thing, the second invention is not new; but if the two things are different, the nature and extent of the differences have to be considered. The question then becomes one of degree. But unless it can be said that the differences are practically immaterial; that there is no ingenuity in the second invention, no experiment necessary to show whether it can be usefully carried out or not, the second cannot be said to have been anticipated by the first
>
> (from *Gadd v. The Mayor, etc., of Manchester* (1892), 9 R.P.C. at 525). (See also *Sharp & Dohme Inc. v. Boots Pure Drug Co. Ltd.* (1927), 44 R.P.C. 367 , (1928), 45 R.P.C. 153 ; *British Celanese Ltd. v. Courtaulds Ltd.* (1933), 50 R.P.C. 270 .

20. More recently, the Federal Court in *Axcan Pharma Inc. v. Pharmascience Inc. et al.* (2006), 50 C.P.R. (4th) 321 applied this approach to anticipation at paras 38 and 52:

> [38] If I had found that a dosage of 13-15 mg/kg/day was not essential to Dr. Poupon's claim, the publication of Dr. David's study would have invalidated the patent. Had the dosage not been essential, then Dr. Poupon's claim could not be differentiated from Dr. David's study.
>
> Y
>
> [52] In the alternative, if the dosage is not an essential element, then the patent is still invalid because a claim for the use of Ursodiol in the treatment of primary biliary cirrhosis was reported in Dr. David's article which was published more than two years prior to the application for the Canadian patent.

21. Further, the courts have held that if a disclosure provides information that would infringe a claim, if it was to be carried into effect after the patent, as a general rule, the disclosure anticipates the same claim, if it was published prior to the claim date. This principle has been applied recently in *Eli Lilly Canada Inc. v. Apotex,* 2008 FC 142 at para. 138 and *Abbott Laboratories v. Canada (Minister of Health)*, 2006 FCA 187 at para. 25, both citing *Lightning Fastener Co. v. Colonial Fastener Co.*, 1933 CarswellNat 43 (S.C.C.), [1933] S.C.R. 377, [1933] 3 D.L.R. 348 [*Lightning Fastener*], wherein it was stated:

> ABut what amounts to infringement, if posterior, should, as a general rule, amount to anticipation, if anterior.@

As the test for infringement permits the omission or substitution of non-essential elements of a claim (*Free World Trust*, *supra)*, it follows that a prior disclosure can omit or substitute non-essential elements and still anticipate a claim.

22. Following the decision in *Free World Trust*, when considering anticipation, the determination of whether a difference between a prior art disclosure and a claim is Apractically immaterial@ is made by an analysis of whether the difference, or variant, is essential or non-essential, in accordance with the principles in that decision. This approach for anticipation is consistent with the approach taken when considering infringement of a claim, ensuring that the Afairness and flexibility@ provided by purposive construction is maintained for questions of both validity, such as anticipation, and infringement.

23. While, indeed, the test for anticipation is a difficult one to satisfy, it is as a result of the necessity for the information to be disclosed in a single, prior, enabling reference that

discloses all of the essential elements.

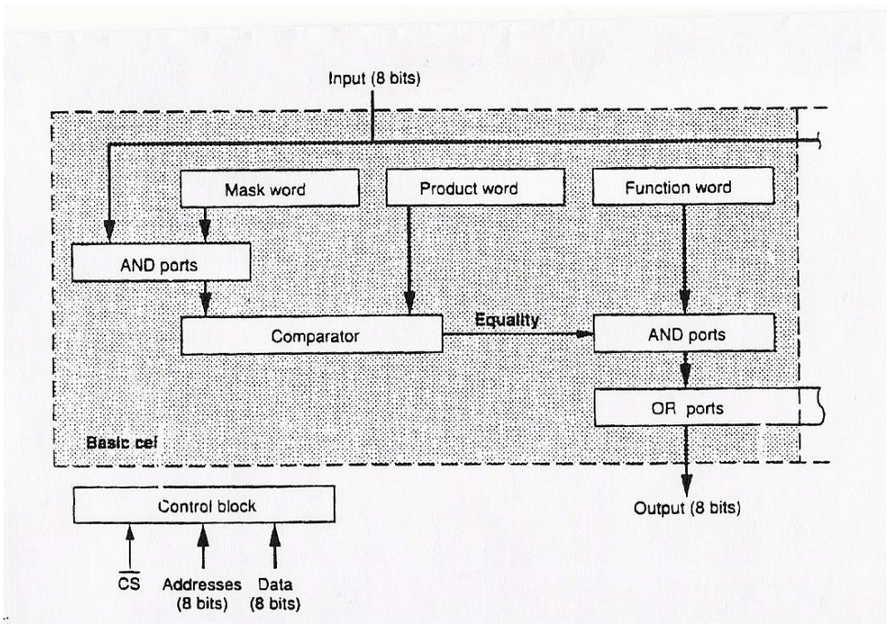
Analysis and Findings: Anticipation

24. The Board has carefully considered the claims and finds that claims 1 to 12 are anticipated by the Dancea[1] publication. The claims will be addressed one at a time, and compared with the information given in Dancea[1].

Overview of Dancea[1]

25. Dancea[1] is the third in a series of three prior disclosures by the Applicant. Dancea[1] has a date of publication which is more than 11 years prior to the filing date of the present application, and presents the Aproduct terms method@, starting at page 41 therein. On page 41 (column 1, 4th paragraph), Dancea[1] states that the described method may be used to implement any multiple output combinational circuit. Dancea[1] extends the product terms method to synchronous sequential circuits. An expert system is proposed to develop tables representing the Boolean equations, including a database for storing and retrieving Boolean equations representing different target circuits. Figure 1 depicts a flowchart of the product terms method illustrating the sequence of operations performed on the three memory words and the input word in order to obtain the logical values of the output functions representing the behaviour of the target circuit. Page 42 provides an example of the method applied to a combinational circuit. At pages 42-43, including Figure 2, Dancea[1] discusses how the method could be used to simulate synchronous sequential circuits such as a Moore sequential circuit. At pages 44-45 and in Figure 9, an example is provided of a synchronous sequential circuit that could be simulated

using an implementation of the product terms method. Figure 9 displays the tables of memory words that represent the combinational circuits that make up the sequential circuit of the example. On pages 45-46, the paper turns to an explanation of the expert system as well as an interface and its driver. Finally, at page 50 and Figure 12, a VLSI circuit is provided to implement the product terms method. The closing paragraphs at pages 50-51 of Dancea[1] highlight that: it can implement combinational and synchronous sequential circuits; the same implementation algorithm is used for all digital structures; and either software or hardware (for example, the proposed VLSI circuit in Figure 12) implements the proposed method. A hardware implementation is suggested for critical-time situations. Figure 12 of Dancea[1] is shown below:



26. To begin our analysis, claims 1 and 12 are method claims and claims 2 to 11 are device claims, although they ultimately depend upon method claim 1.

Claim 1: Analysis and Findings

1. A computer assisted method for changing the logical behaviour of a dynamically re-configurable VLSI device from one target circuit to other target circuit, comprising an interface which allows to receive a configuration or reconfiguration request, a peripheral adapter for managing the configuration processes and an expert system, and further comprising the steps of:

(a) receiving a configuration or re-configuration request from a user or a running program to configure or to re-configure the said VLSI device to a target circuit defined by one or several groups of sum-of-product logical equations; and

(b) configuring or re-configuring the said VLSI device by the said expert system to processes the sum-of -product logical equations.

27. The Board has identified that pages 15-16, pages 19-20 and Figures 5 and 10 of the original description dated February 27, 2001 provide some support for this method claim. With respect to the interface and peripheral adapter in the preamble, the Board has considered the ordinary and technical sense of these words in the art. The context of its use in the claim suggests that the interface interacts with the expert system. This is consistent with page 15 of the description wherein a user Ainterrogates an expert system@, and Figure 5 and element 81 in Figure 10. In view of step (a) of claim 1, Areceiving... a request from a user or a running program@ and page 16 (lines 5-8), the interface can either comprise an interface with a user (Auser interface@), or an interface with a Acontrol program@.

28. As for the peripheral adapter, one is left to wonder what the scope of this term is intended to include, however, the claim states that it is something provided for Amanaging the configuration processes@. Pages 15 and 16 of the description and Figure 5 indicate that

the peripheral adapter functions to configure or update the appropriate registers of the VLSI chip. The registers embody one or more tables containing the memory words, the tables being employed to configure or re-configure the circuit structure (page 20, lines 6-7; Figure 10, step 86).

29. The Board notes that the details of both the interface and peripheral adapter are evidently left to the person skilled in the art to design and implement, given the lack of description and literal or substantive support thereof. The remainder of this method claim appears to be reasonably supported by the description and drawings.

30. Turning to Dancea[1], an expert system is disclosed to program an implementation (neither software nor VLSI is specified) of the product terms method (see pages 43-46, Dancea[1]). A specific example is shown in the context of a software implementation of the product terms method under the heading AA real interface and driver@ at pages 46-48 (Dancea[1]) and its associated Figures. In this example, the product terms algorithm is implemented in software running on a PC. In particular, Figure 8 includes Acalls to the algorithm of the product terms method@. While there is no explicit discussion of using the expert system to configure a VLSI circuit implementation of the product terms method within Dancea[1], the Board is of the opinion that a skilled person reading the described expert system would understand it can be used with any implementation of the product terms method, including a VLSI device as defined on pages 50 and 51 and Figure 12 of Dancea[1]. As for enablement of the configuration method disclosed in Dancea[1] in the context of a hardware (VLSI) implementation of the product terms method, it is noted that everything within the present description that enables claim 1, is found in Dancea[1]. This leads to the deduction that Dancea[1] provides sufficient

information to one skilled in the art in such a manner that step (b) of configuring Athe said VLSI device by the said expert system to process the sum-of -product logical equations@ is disclosed.

31. Claim 1 recites an interface which receives a configuration request. This is described by Dancea[1] where the expert system Ainteracts with the user...@ to offer a choice of either entering Boolean equations that describe the behaviour of a circuit, or to select a prestored structure from a database (see Dancea[1]: page 43, lines 29-35; Figure 3). In response to the selected choice, the expert system ultimately transfers the table representing the user=s selected circuit to a driver controlling the interface (hardware interface, not the user interface with the expert system), thereby affecting the requested configuration (Dancea[1]: page 46). This is clear direction to a person skilled in the art to employ the expert system to carry out the step (a) in claim 1 of Areceiving a configuration or re-configuration request from a user or a running program to configure or to re-configure the said VLSI device to a target circuit defined by one or several groups of sum-of-product logical equations@; and step (b) in claim 1 of Aconfiguring or re-configuring the said VLSI device by the said expert system to processes the sum-of -product logical equations.@

32. The Board concludes that the peripheral adapter comprises the driver and the associated hardware interface described at page 46 and Figure 6 in Dancea[1]. The expert system is discussed in as much depth in Dancea[1] as it is in the Applicant=s original description, at pages 43-45 and its associated Figures.

33. In light of the above, the Board finds that Claim 1 is anticipated by Dancea[1] .

Claim 2: Analysis and Findings

> 2 A dynamically re-configurable VLSI device as recited in claim 1 for implementing combinational circuits defined by a group of sum-of-products logical equations, comprising:
>
> "m" input terminals connected to an input register for storing the input variables;
>
> "n" cells, a cell C(k) for determining a logical value of a product term p(k) of said logical equations corresponding to said input variables, where "k" is an integer k [1 ,n]; and
>
> a block of "r" OR gates, each gate having "n" inputs, connected to said cells C(k) for receiving said logical value of said product terms p(k) and providing a logical value for each said logical equations at Ar" output terminals.

34. The claim recites OR gates for "receiving said logical value of said product terms p(k)". This appears to encompass inoperable embodiments in light of the present description (page 7, last paragraph; page 11, second last paragraph; and, page 14, first paragraph). While a single-output embodiment does include an OR gate which receives the logical values of the product terms, multiple output embodiments do not. The OR gates of multiple output embodiments receive a bit of each function word of each product term, and not the logical values thereof, when a given product term is "active". This leads to a significant difference in that when the function word is forwarded, the bit thereof sent to the OR gate of an output equation to which the product term does not contribute will be 0 rather than the logical value 1. For the purposes of analysing anticipation and obviousness, the Board will read-in that the OR gates receive respective bits of the function words when the logical value of a product term is 1, and receive a 0 from product

terms whose logical value is 0. If a patent were to grant on this application, this defect would need to be addressed.

35. Referring to Figure 12 of Dancea[1], it includes Am@ input terminals, An@ cells, and AOR ports@ which provide Ar@ output terminals, wherein Am@, An@, and Ar@ are undefined values. Preferably, the Examiner should have addressed the following elements as well: that Dancea[1] discloses an input register; multiple C(k) cells; that each cell in Figure 12 determines the logical value of a product term; and that the OR gates in Figure 12 each have An@ inputs connected to the cells for providing a logical value for each of the output equations at the output terminals.

The input register

36. The input register serves to store the input variables and is connected to the input terminals. Although not recited in the claim, the input terminals supply the logical values of the input variables from the input register to each basic cell (description: page 13, lines 14-17; Figures 3 and 4). A detailed reading of the specification shows that there is no requirement to store the input variables. It is only necessary that the input values be supplied to the basic cells. The manner in which the input values are supplied to the input terminals, and ultimately to the basic cells, has no bearing on the performance of the claimed VLSI device.

37. Figure 12 of Dancea[1] depicts a single basic cell and not the entire VLSI device. In that Figure, the input variables are supplied to the illustrated cell via input terminals. The Figure does not show how the input variables are supplied to the input terminals of the cell, whether it is from an input register or not.

38. The input register in this case is very similar to the elements found to be non-essential in *Free World Trust*, where at paragraph 20 the Supreme Court stated:

> Based on the expert evidence given at trial as to the meaning of the terms used, and the understanding that these terms would convey at the date of the patent to an ordinary worker skilled in the art of electromagnetotherapy devices and possessing the common knowledge of people engaged in that field, it appears that while some of the elements of the '156 and '361 patents are essential if the devices are to work as contemplated and claimed by the inventor, others are non-essential. The non-essential elements may be substituted or omitted without having a material effect on either the structure or the operation of the invention described in the claims.

And at paragraph 23:

> The '156 patent includes a number of additional claims dependent on claim 1. Thus, for example, claims 4 and 5 claim a "repeatedly discharged capacitor"
> ...
> the evidence is that much of this equipment is commonly used in university science laboratories and in other settings involving the production of magnetic fields using electric currents through coiled wires. They are included in the patent only because of their use in conjunction with "essential" elements of the invention described in claim 1. In the case of some of these specific components, anyone skilled in the art reading the patent at the date of its publication would immediately have appreciated that there existed different commonly-known substitutes or mechanical equivalents that would do the job just as well. The claims of the ' 361 patent also contemplate a number of interchangeable components that do not constitute part of the essential invention. Thus, claims 5, 14 and 20 of the '361 patent refer to the use of switches in conjunction with the device described in claim 1. These components themselves were not patented on their own -- indeed, they could not be patented since they represent equipment commonly known and used by persons skilled in electrical engineering. They came to be included in the claim as an element of an ingenious combination. Substitution of one type of switch for another in this case would not strike at the essentials of the invention.

Further on, at paragraph 55, the Court described the principles in determining whether an element is non-essential:

> For an element to be considered non-essential and thus substitutable, it must be shown either (i) that on a purposive construction of the words of the claim it was clearly not intended to be essential, or (ii) that at the date of publication of the patent, the skilled addressees would have appreciated that a particular element could be substituted without affecting the working of the invention...

39. The Board is satisfied that the skilled workman would have appreciated that omission of the input register, so long as input terminals are provided, would not materially affect the way the invention operates and may therefore be considered as non-essential. Omission of the input register would not strike at the essentials of the invention. The VLSI device would continue to operate in the same way, performing the same function and provide the same result (*Free World Trust, supra)*.

40. Accordingly, though an input register would likely have been included by the skilled person in attempting to construct a VLSI device in accordance with the teachings of Dancea[1], it is not required to be found in that publication for a finding of anticipation.

Multiple C(k) cells

41. It is clear that before the claim date, a skilled person reading Dancea[1] would have known that a VLSI implementation would require several C(k) cells (basic cells), to achieve its objective. First, each product term in the product terms method requires a single mask word, product word, and function word. The basic cell shown in Figure 12 of Dancea[1] includes a register for each of the three words. Thus, the illustrated single basic cell is provided to compute the value of a single product term (see also page 41: Figure 1; column 2, lines 5-12). Since Dancea[1] presents Figure 12 in the context of the "idea of parallel processing of product terms" (page 50 of Dancea[1]), the Board is satisfied that multiple basic cells would be consistent with this teaching, and thus necessary. While Figure 12 only shows the details of a single basic cell, further cells in Dancea[1] are illustrated by the continuation of both the OR ports and the input terminals beyond the basic cell (see right-hand side of the figure). Further, the presence of multiple cells in

Dancea[1] is confirmed by the Applicant on page 3 of the letter dated October 21, 2002 where he states that 5 product terms in Dancea[1] will require 5 cells.

Each cell determines the logical value of a product term

42. As for the requirement in claim 2 that each cell determine the logical value of a product term, as explained above, the arrangement of the basic cell of Figure 12 is provided to determine the logical value of a single product term. A sequence of operations is performed on the input variables using the three words in order to determine the logical value of the product term. As stated at page 50 of Dancea[1], "the combinational part of the cell acts as a filter between the product term information and the outputs". Thus, each cell in Dancea[1] determines the logical value of a single product term.

Ar@ OR gates, each having n inputs connected to the basic cells, for receiving a logical value of said product terms, and to provide a logical value for each of the output equations at Ar@ output terminals

43. The connectivity of the OR gates (shown as OR ports) in Figure 12 of Dancea[1] is not shown. The drawing of the OR port (Figure 12, bottom right) extends beyond the basic cell into adjacent cells. This is consistent with the product terms method described in Dancea[1]. In particular, the logical equation for each output function is in the form of "sum of products" (Dancea[1]: page 41; page 42, example). That is, the logical value of the output function is expressed in terms of the sum of the product terms. In Boolean algebra, summation is provided by the "OR" operator. To obtain the summation of the product terms of an output function, each product term must be "OR"ed with one another.

Therefore, the logical value of each output function is computed by a single AOR@ gate, having the product terms as its input.

44. Thus far, it is useful to summarize that the Board has established that the following would be readily understood by those skilled in the art reading Dancea[1]: each basic cell (Figure 12) determines the logical value for a single product term; Aparallel processing of product terms@ (page 50, column 2, line 4) directs the skilled person to employ multiple basic cells to implement multiple product terms in parallel; the drawing of the OR port (Figure 12, bottom right) points to an OR operation which accepts inputs from outside the cell or neighbouring cells; and the product terms must be AOR@ed with one another at a single OR gate for each output function, to achieve summation of product terms.

45. The Board is of the opinion that a skilled technician reading Dancea[1], by virtue of his skill in logic design, would immediately realize the appropriate connections within the VLSI device by using the single basic cell of Figure 12 as a building block. A product terms method implementation providing an 8 bit output, consistent with Figure 12, would have 8 OR gates, with the inputs to each of those OR gates connected to the AND ports from the basic cells, so as to achieve parallel processing of the respective outputs from the AND ports (from each basic cell). Thus, one skilled in the art following the instructions of Dancea[1], would have implemented parallel processing of product terms by feeding, respectively, each most significant bit (MSB) from the AND ports of each basic cell into the same OR gate, each MSB-1 bit from the AND ports of each basic cell into another OR gate, each MSB-2 bit from the AND ports of each basic cell into yet another OR gate, and so on. In this manner, Ar@ output terminals would be provided by Ar@ OR gates, each OR gate having An@ inputs (where An@ is the number of basic

cells needed for a given VLSI device implementation). One would not deliberately constrain the design of the device by providing only some of the basic cell outputs to certain OR gates. The result would be to limit the number of product terms for a given output function. This would be contrary to the object of the disclosure in Dancea[1] to implement Aany multiple output combinational circuit@ (p.41) and for Athe same hardware structure to implement a large number of circuits@ (p.51).

46. Thus, the Board concludes that a device implemented by following Dancea[1], must be: a block of "r" OR gates; each gate having "n" inputs connected to said cells C(k), for receiving said logical value of said product terms p(k) and providing a logical value for each said logical equations at "r" output terminals. The Board is unable to conclude, as suggested by the Applicant in his letter dated October 21, 2002, that Dancea[1] teaches the use of three OR gates in each cell if the term aANDb is present in all three equations. It is unclear as to what useful purpose such a structure would serve in Dancea[1].

47. Consequently, the Board has determined that the Dancea[1] reference (in particular: Figure 12 and the associated description) conveys enough information to lead a skilled person to the subject matter in claim 2, without the exercise of inventive skill, and without possibility of error.

48. The Board has also considered the statements on page 5 of the Applicant=s letter dated January 21, 2002 regarding Figure 12 in Dancea[1], in particular:

> Furthermore, no correct specifications exist in the mentioned Figure 12 (publication Dancea[1]) concerning the circuit parameters and their function, precisely the number of inputs m, of outputs

r and of product terms p(k). These parameters establish the performance limits. Instead, a non-justified value of 8 inputs and 8 outputs is shown. In addition, the Figure 12 (publication Dancea[1]) and the attached text do not give any indication concerning the number or type of equations (outputs or next state) that the circuit implements.

49. The Board notes that the parameters m, r, k in claim 2 are not explicitly stated in Dancea[1], in a literal sense. However, claim 2 does not set forth any distinguishing features pertaining to the number or type of equations the circuit implements. There are also no performance limits placed on the device of claim 2 by the parameters m, r, and k. As a result, further consideration of these parameters does not save claim 2 in the situation where it reads on Dancea[1] when appropriate values are assigned to m, r, k and n. The lack of performance limits or distinguishing features in claim 2 regarding these parameters, leads the Board to conclude that these values do not materially impact the way the alleged invention works.

50. In view of the above, the Board finds that claim 2 is anticipated by Dancea[1].

Claim 3: Analysis and Findings

3 A dynamically re-configurable VSLI [sic] device as defined in claim 2, wherein said cell C(k) comprises:

a registers storage area for storing a mask word, a product word and a function word, representative of said product term p(k);

first logic level means for receiving said "m" input variables and logical values of said mask word to generate intermediate results;

second logic level means for comparing said logical values of said product

word with said intermediate results to determine said logical value of said product term p(k); and

third logic level means for transferring said function word to said "r" output terminals, according to said logical value of said product term p(k).

51. The registers storage area is disclosed in Figure 12 and its associated description on page 50 of Dancea[1], which describes Athree one-word registers that store the mask word, the product word, and the output word [function word] of a logical product [product term]@. These features are clearly representative of a product term as the product term method requires a set of each of the three words for each product term (as discussed in the analysis of claim 2, above).

52. The Afirst logic level means@ in claim 3 are provided by the first set of AAND ports@ in Figure 12 of Dancea[1] shown on the left side of the cell. The AND ports receive the input variables and mask word to produce an intermediate result.

53. The Asecond logic level means@ is provided in Figure 12 of Dancea[1] by a comparator block that evaluates the product word against the intermediate result from the Afirst logic level means@ to provide the logical values of the product term.

54. Before considering the "third logic level means", the Board notes that claim 3 is inconsistent with the description (pages 9, 13, Figures 3-4) in that it provides for the transferring of the function word directly to the output terminals. According to the product terms method, as taught in the description of the present invention and in Dancea[1], the function word must be "OR'ed" with the function word of all other product terms (to yield

the final summation required in the sum-of-products form of the output equation). The claim omits logic that is essential to ultimately determine the logical value of the output functions. For the purposes of anticipation and obviousness, the Board will read-in the requirement for the function word to be forwarded to the inputs of the block of "r" OR gates of claim 2. However, if a patent were to issue on this application, this defect would need to be addressed.

55. For the Athird logic level means@, Figure 12 of Dancea[1] includes a second block of AAND ports@ on the right hand side of the cell, and "OR ports". The comparator output (i.e., the logical value of the product term) and the function word are supplied to the AND ports. The AND ports forward the function word to the OR ports when the comparator provides a logic 1 (equality). This latter detail is not explicitly shown in Figure 12 as the wiring of the gates is abstracted out of this block diagram. However, the forwarding of the function word when Aequality@ is obtained is inferred from an understanding of the product terms method and its algorithm. One skilled in the art would have implemented the VLSI circuit shown in Figure 12 of Dancea[1] by arranging the inputs to the second block of AND gates to provide the function word as the output thereof when the comparator supplies an Aequality@ signal thereto (i.e., according to the logical value of the product term). The "third level logic means" of Dancea[1] transfers the function word to the OR port, the output thereof providing the output terminals.

56. The Board finds that Claim 3 is anticipated by Dancea[1]. As in the case of claim 2, this finding is further reinforced by the fact that there are no bounds on m, n, k, and r, so that when suitable values are chosen, the structure in claim 3 is seen to be anticipated by Dancea[1].

Claim 4: Analysis and Findings

> 4 A dynamically re-configurable VSLI [sic] device as defined in claim 3, wherein said registers storage area comprises two m-bit registers and one r-bit register.

57. The composition of the register storage area is not explicitly shown in Figure 12 of Dancea[1]. Although the Final Action labels these features as Afurther details of internal arrangements@ and Anecessary logic for determining product terms@, it would have been preferable for the Examiner to elaborate on these statements.

58. From an understanding of the product terms method, and in particular the description of the three words at column 2 of page 41 in Dancea[1], the mask word and product word both contain one bit per input variable (as they both represent associations related to the input variables). From dependant claim 2, Am@ represents the number of input variables. It follows that the mask and product word registers shown in Figure 12 are "m" bits wide ("m" = 8 in the example, as the input is 8 bits wide) and therefore read on this element of the claim. Similarly, the function word is known, from page 41 (called output word) and the example disclosed on page 42 of Dancea[1], to require as many bits as there are outputs (output equations). As "r" in the claims, from dependant claim 2, designates the number of output terminals, it follows that the function word register of Figure 12 in Dancea[1] is "r" bits wide (where "r"=8, as the output in that example is 8 bits wide).

59. The Board finds that Claim 4 is anticipated by Dancea[1].

Claim 5: Analysis and Findings

> 5 A dynamically re-configurable VSLI [sic] device as defined in claim 3, wherein said first logic level means comprises m*(2-bit) AND gates, each one for receiving a respective bit of said "m" input variables and of said mask word to produce a respective bit of said intermediate result.

60. While the m*2 bit configuration of the AND gates for the Afirst logic level means@ is not explicitly shown in Figure 12 of Dancea[1], it is clear that the first AAND port@ receives an 8 bit input and would undergo a bit-wise AND operation with 8 bits of the mask word. As explained earlier with reference to claim 4, Figure 12 follows the situation where m = 8, including either a m or 8 bit mask word. The Board is of the opinion that any skilled person reading the disclosure of Dancea[1] and interpreting Figure 12 would understand that if the input was 16 bits (i.e. m = 16), the AND port would require a 16*2 bit AND port, each 2 bit gate for accepting the input bit plus the mask word bit.

61. The Board finds that Claim 5 is anticipated by Dancea[1].

Claim 6: Analysis and Findings

> 6 A dynamically re-configurable VSLI [sic] device as defined in claim 3, wherein said second logic level means comprises:
>
> m*(2-bit) XNOR gates, each one for receiving a respective bit of said intermediate result and of said product word to provide a bit of comparison result;

and

a (m-bit) AND gate for receiving "m" bits of said comparison result to provide said logical value of said product term p(k).

62. Claim 6 specifies m*(2-bit) XNOR gates to compare the intermediate result with the product word. The XNOR gates are also referred to as AEQUIVALENCE@ gates throughout the specification, and their use is frequently referred to as a Acomparison operation@ (original description: page 7, lines 26-27; page 11, lines 14-18; page 13, lines 24-29). The output of the XNOR gates is supplied to a single AND gate. The output of the AND gate provides the logical value of the product term.

63. A notable excerpt from page 11, lines 14-18 of the original description dated February 27, 2001 states:

> These intermediate results are obtained by EQUIVALENCE operations, which gives logic 1 when both bits are identical (i.e. both are logic 0 or logic 1) and gives a logical 0 when the bits are different, i.e. one is logic 0 and the other is logic 1 (EQUIVALENCE AND [XNOR] express the same logic operation).

64. Figure 12 of Dancea[1] shows a comparator which takes the intermediate result (from the AND port) and the product word as inputs, and has as its output a signal called AEquality@. The details of the comparator circuit are otherwise abstracted out of the Figure, leaving further implementation details to the skill of the reader.

65. Since Figure 12 also has an equality (i.e. equivalence) operation, the Board is satisfied that the comparator block in Figure 12 of Dancea[1] provides the same functionality as the

XNOR gate in claim 6. A skilled person reading Dancea[1] would have understood that comparators are implemented as XNOR gates.

66. On page 3 of the Applicant=s response dated October 21, 2002, it is stated:

> In reality, with standard outputs for every basic cell, saying 8 or 16 outputs, and with several hundreds of product terms, the excess of OR gates, and the presence of the comparator in Dancea[1] publication instead of XNOR gates, multiply by several orders the number of gates found in the architecture of the proposed VLSI circuit of the patent application.

67. The Board does not agree, as alluded by the Applicant, that the comparator required in Dancea[1] would be understood by the skilled technician to be implemented with excess gates (beyond the XNOR gates required for the equivalence evaluation). The Applicant appears to be suggesting that the skilled technician would have implemented a more complex variety of comparator, such as a magnitude comparator. The skilled technician would not employ such a structure as the logic for evaluating Agreater than@ and Aless than@ conditions are not required. The skilled technician would have implemented a comparator that solely conducts an equivalence (=) evaluation, as required by Dancea[1].

68. With respect to the provision of m*(2-bit) for the XNOR gate, and m-bit for the AND gate, as explained earlier, the Board is of the opinion that specifying Am@ scalability would be known on the claim date to a person skilled in the art to not materially affect the operation of the basic cell found in Figure 12 of Dancea[1]. The Board earlier demonstrated for claim 4 that having the m*(2-bit) configuration is shown in Dancea[1] for the registers and AAND@ gates, and therefore this configuration also applies for the XNOR gates.

69. The Board finds that claim 6 is anticipated by Dancea[1].

Claim 7: Analysis and Findings

> 7 A dynamically re-configurable VSLI [sic] device as defined in claim 3, wherein said third logic level comprises: r*(2-bit) AND gates to allow transfer of said function word if said product term p(k) has the logical value 1.

70. This claim recites further details of the Athird logic level means@ of claim 3. The lower right hand part of Figure 12 in Dancea[1] discloses AND gates (shown as AND ports). They permit the transfer of the function word from its register when an equality signal is received from the comparator. The only question here is whether the AND block comprises Ar@ 2-bit gates. In analysing claim 2, the Board concluded that the OR port would require the same number of Ar@ OR gates as desired Ar@ outputs, when Figure 12 is read by a person skilled in the art. In claim 2, the Board also determined that each bit of the output is obtained by performing an OR operation on a number of inputs equal to the number of basic cells used (in claim 2, n = number of basic cells). Further, with respect to claim 4, it was shown that the function word of Dancea[1] requires one bit for each possible output function. As there are "r" bits in the function word, it follows that "r" AND gates are required if the equality signal is to be used to forward the function word. Thus, with respect to claim 7, a skilled technician reading Dancea[1] would realize that the AND port has r outputs and must have r AND gates. Since the AND operation has two inputs, one from the function word, and one from the equality, the AND port in Figure 12 consists of r*2-bit AND gates. The Board concludes that Ar@ 2-bit AND gates

are implied in Figure 12, if the equality signal is operative to forward the function word.

71. In view of this, the Board finds that Claim 7 is anticipated by Dancea[1].

Claim 8: Analysis and Findings

> 8. A dynamically re-configurable VLSI device as defined in claim 1 for implementing a circuit defined by a single sum-of-products logical equation, wherein said VLSI circuit comprises a single OR gate connected to the said n cells for receiving said logical values of said product terms p(k) to provide a single output for said logical equation.

72. Unlike device claims 2 to 6, this claim depends directly on claim 1. Claim 1 does not impart any device limitations to this claim. The claim is directed to a Asingle output@ device wherein the logical behaviour of the target circuit must be described by a single equation. It recites a very limited re-configurable VLSI device and, accordingly, its design is less complex. Claim 8 requires a single OR gate connected to An@ cells which receives the logical values of the product terms to provide a single output.

73. The disclosure of the VLSI circuit in Dancea[1] shows an AOR ports@ block with an 8-bit output, representing a maximum of 8 output functions to be evaluated. One skilled in the art would understand that the AOR ports@ block would require 8 OR gates in order to provide an 8 bit output. While this particular embodiment does not precisely read upon the present claim, the embodiment of Figure 12 of Dancea[1] is only an example. The publication provides clear direction and enablement to produce a VLSI circuit implementing the product terms method with any number of output bits, including a single

bit. The OR ports block would include as many OR gates as there are output bits (as discussed with respect to claim 2). For an embodiment comprising a single output bit, a single OR gate would be provided. Dancea[1] teaches that the function word is provided to Aindicate the contribution of the product term to the outputs@. This would have lead the skilled person to realize that the function word would not be required in a single output embodiment. Thus the skilled person would not have employed an AAND ports@ block. The equality signal, representing the logical value of the product term, would be supplied to the AOR ports@, which would comprise a single OR gate. Thus, Dancea[1] provides information that gives the subject matter of this claim.

74. The Board concludes that Claim 8 is anticipated by Dancea[1].

Claim 9: Analysis and Findings

> 9 A dynamically re-configurable VSLI [sic] circuit as defined in claim 8, wherein said cell C(k), comprising:
>
> a storage area for storing a mask word and a product word, representative of said product term p(k);
>
> first logic level means for receiving said m input variables and logical values of said mask word to generate intermediate results; and
>
> second logic level means for comparing said logical values of said product word with said intermediate results to determine said logical value of said product term p(k).

75. In view of the analysis and findings of Claim 3 (with respect to the disclosure of first and second logic level means in Dancea[1]) and Claim 8, upon which this claim depends, the

Board finds that claim 9 is anticipated in view of Dancea[1].

Claim 10: Analysis and Findings

> 10 A dynamically re-configurable VLSI circuit as defined in claim 1, for implementing synchronous Moore sequential target circuits with clock input only, wherein said input register is a state register for storing "s" state variables defining a current state, said VLSI circuit further comprising:
>
> a clock input for changing the content of said state register from a current state to a next state;
>
> a feedback connection from said Ar" outputs of said OR gates to said state register.

76. This claim is directed to a synchronous sequential circuit implemented by a VLSI implementation of the product terms method. It is noted that this claim depends upon claim 1, which does not impart any device limitations through the dependancy. As such, there is no structure recited in this claim aside from a VLSI circuit that comprises a clock input, an input register that is a state register, and a feedback connection. This claim is deficient in many ways beyond the question of whether or not it is anticipated.

77. Dancea[1] discloses the use of the product terms method to implement synchronous Moore sequential circuits. Dancea[1] also discloses a VLSI implementation of the product terms method. Figure 12 of Dancea[1] is directed to a VLSI implementation configured to implement combinational target circuits and could not, as shown, implement sequential circuits. However, the skilled reader understands the design of Moore sequential circuits. A Moore sequential circuit includes a combinational circuit that provides an

output that depends only upon the present Astate@ of the circuit (see Figure 1 APrior Art@ of description; and Dancea[1], page 42, second column and Figure 2). The state is defined as the binary information stored in storage elements, such as registers, at an instant in time. A synchronous circuit is one that includes a Aclock signal@ which serves to effect storage elements, such as registers, at discrete instants in time. Evidently, the combination of the VLSI implementation of the product terms method, the disclosure of the product terms method being suitable to implement synchronous Moore sequential circuits inevitably leads to the claimed subject matter. The Dancea[1] reference is to be read by the skilled reader. The skilled reader necessarily reads into the terms Asynchronous Moore sequential circuit@ the elements recited in this claim.

78. As such, the Board finds that claim 10 is anticipated in view of Dancea[1].

Claim 11: Analysis and Findings

11 A dynamically re-configurable VLSI circuit as defined in claim 1 for implementing synchronous Moore sequential target circuits with clock input and with Am" data inputs, comprising:

a register for storing Am" input variables;

a state register for storing "s" state variables;

a first combinational circuit defined by a first group of sum-of-product equations, said first combinational circuit including N1 cells C(k) as defined in claim 3, for receiving "m@ inputs and "s" state variables, and having "r1" outputs;

said clock input for changing the content of said state register from a current state to a next state;

a feedback connection from said "r1" outputs of said first combinational circuit to said state register; and

a second combinational circuit defined by a second group of sum-of-product equations, said second combinational circuit including N2 cells C(k) as defined in claim 3, for receiving said next state variables and providing final "r2"outputs.

79. This claim is also directed to a configurable VLSI device for implementing synchronous Moore sequential circuits.

80. Both Figure 2 of Dancea[1], and Figure 1 (prior art) of the present application, show all of the recited elements of claim 11. Dancea[1] teaches that the product terms method can be used to implement combinational or synchronous sequential circuits, and that the method may be implemented with a VLSI circuit. The details of designing a VLSI circuit for implementing synchronous Moore sequential circuits are not provided explicitly, however, the general layout of such Moore circuits is shown at Figure 2 of Dancea[1]. Looking to Figure 2, the state-register is depicted as Aflip-flops@; first combinational circuit is shown as Acombinational circuit 2", receiving inputs (shown) and state variables (represented by the arrow pointing from the Aflip-flops@ to the Acombinational circuit 2"); the feedback connection is shown as the arrow pointing from the Acombinational circuit 2" to the Aflip-flops@; and the second combinational circuit shown as Acombinational circuit 1" which receives the next state (represented by the arrow from the Aflip-flops@ to the Acombinational circuit 1") and provides final outputs (shown as Aoutputs@). It should be noted that Aflip-flops@ are the actual binary storage elements found within registers. Each bit stored in a register is stored in a single Aflip-flop@. The collection of flip-flops provides the storage capacity for a register.

81. The Board is satisfied that Dancea[1] provides a VLSI circuit for implementing combinational circuits at Figure 12. Thus, the skilled reader would be lead directly, without possibility of error, to substitute the VLSI circuit of Figure 12 in place of the combinational circuits (that form the sequential circuit) shown in Figure 2 of Dancea[1].

82. The Board concludes that claim 11 is anticipated in view of Dancea[1].

Claim 12: Analysis and Findings

12 A computer method as recited in claim 1, where said expert system program, which receives a configuration or re-configuration request and processes the sum-of-product logical equations defining the logical behaviour of a target circuit comprises:

means for selecting the type and functionality of said VLSI circuit;

means for inputting variables names associated with said logical equations;

means for inputting variables names associated with said logical functions;

means for inputting said logical equations;

means for detecting syntactic errors of said logical equations;

processing means for calculating a mask word, a product word, and a function word for each product term p(k) of said logical equation;

means for arranging said mask, product and function words in equation lists, each equation list corresponding to a logical equation;

means for generating a behavioural list; and

loading said behavioural list in registers storage area of said cells C{k) as defined in claim 3.

83. As stated earlier, the Board interprets this claim as a method claim. It recites a number of Ameans@ to further define the expert system introduced in method claim 1. The Board finds that the use of an expert system as described in claim 12 has been shown in Column 1 and Figure 3 on page 43 and Figure 4 on page 45 of Dancea[1]. As shown in reference to claim 1, Dancea[1] provides all of the information needed for a skilled person to design a system to select the type and functionality of a VLSI circuit; input variable names associated with logical equations and functions; input logical equations; detect syntactic errors in logical equations; calculate a mask word, product word, and a function word for each product term; and arrange them in equation lists.

84. With respect to generating a behavioural list, and loading the behavioural list into the registers of the cells, while Dancea[1] does not explicitly recite this, Dancea[1] gives information that inevitably leads to its execution. As discussed in the analysis of claim 1, Dancea[1] teaches the use of the expert system to configure implementations of the product terms method. As the product terms method may be implemented as a VLSI circuit, the skilled reader is provided with information that leads to the use of the expert system to configure a VLSI circuit implementation. This would inevitably require the loading of the memory words into the registers of the cells in order to configure the circuit to implement a target circuit. Thus, the method defined by claim 12 is anticipated by Dancea[1].

85. With respect to the means statements, Figures 3 and 4, and their descriptions in Dancea[1], disclose all of the means recited in claim 12.

86. As such, the Board finds claim 12 to be anticipated by Dancea[1].

Other arguments raised by the Applicant

87. In correspondence with the office, the Applicant argued that the proposed VLSI hardware in Dancea[1] is inadequate and has several logical and conceptual errors. Much of the Applicant=s discussion in response to the Examiner=s objections related to the method of synthesis, the location of the OR gates in Figure 12 of Dancea[1], and the provision of a control block in Dancea[1].

88. These arguments did not affect the findings of the Board for the following reasons.

Ports and Gates

89. Figure 12 of Dancea[1] refers to blocks of AND ports and OR ports whereas the present claims require the use of AND gates and OR gates. The Applicant argued that ports are not the same as gates and that ports are more complicated than gates. In the Applicant's letter dated January 21, 2002, on page 5, he states:

> "The third type of errors in the schema of Figure 12 (publication Dancea[1]) is the presence of terms >AND ports' and >OR ports' instead of >AND gates' and >OR gates'. The applicant mentions that a port is a controlled pathway. To be handled, the port owns its self-control gates. At the time when the article was written, the applicant supposed that the transfer through AND and OR blocks must be validated by control signals, as it happens when the machine language instructions are executed. For this reason, the applicant introduced the terms >ports' and the applicant added in the schema of Figure 12 (publication Dancea[1])

> the Acontrol block@. This block had the role to send the control signals through ports to validated the flow of information. In the patent application solution, the applicant uses gates and not ports because, after simulations, the application observed that the solution is less complex and more secure."

90. In his letter dated October 21, 2002, he states at page 3 [emphasis by Applicant]:

> AIn the previous correspondence the applicant mentioned that: "At the time when the article Dancea[1] was written, the applicant used the term "ports" instead of the term "gates" because he supposed that the transfer through AND and OR blocks must be validated by control signals, as it happens when the machine language instructions are executed by a processor". At hardware level there is no physical difference between ports and gates, both are physical gates. The difference implies the input signals. Conventionally, when it is necessary to make a difference in the design, the inputs of a gate are only data signals, while the inputs of a port are data signals and control signals. Consequently, the applicant wanted to emphasize the fact that **between the solution proposed in Dancea[1] publication and that proposed in the patent application exists an internal hardware difference.**@

91. The Board takes the position that even if the blocks of "ports" depicted in Dancea[1] are in fact intended to represent a more complex structure than a block of AND or OR gates, they certainly include within them, as a subset thereof, the respective gates. Thus the Dancea[1] reference still discloses something within the claims. Furthermore, the Board believes that the skilled reader would take "ports" to mean "gates" and nothing more. The Board is not persuaded that a skilled reader would see any requirement for control signals for validation. The transfer of data from registers through a combinational circuit

to produce an output was a routine matter as of the claim date. The skilled reader would not see any need to provide control signals on the combinational portions of the circuit, nor would the skilled reader interpret the term "port" in the manner the Applicant suggests. Given the method the circuit is to implement (i.e. the product terms method), and the state of the art of digital design at that time, the skilled reader would interpret "ports" to mean "gates".

92. While not relied upon by the Board, this opinion appears to be substantiated by the Applicant's own submission to the USPTO in his Information Disclosure Statement dated June 6th, 2001. Specifically, in describing the "OR ports" in Dancea[1], he described them as "really OR gates". Subsequent discussion of the same block therein refers to "gates" and not "ports". He later states at page 2, paragraph "c" that labelling these blocks as "ports" was in error:

> ". . . the word >ports', which refer to input/output communication and consequently to specific hardware structure, was used throughout the block labelling of Figure 12, instead of the word gates, fact (sic) that is incorrect and can produce confusions (sic)."

93. These statements are completely at odds with the Applicant's submissions to the Examiner on this point. While these statements did not assist the Board in reaching its conclusion, they certainly reinforce its correctness.

94. The Board concludes that the term Aports@, in the sense used in Dancea[1], is equivalent to Agates@.

Location of OR gates

95. The Applicant also states that the VLSI circuit of Dancea[1] was different by arguing that the OR gates were moved from inside the basic cells to the outside thereof. He further argues that the connectivity of the OR gates differs, stating that the OR gates are not connected to the output of each of the basic cells. The Applicant has stated that these differences cause erroneous results in the applied reference.

96. The Examiner pointed out to the Applicant that the OR gate location (in or out of the cells) does not bear any relevance to the claims on file. The Board agrees. Claims 2, 8, and 10 recite OR gates. Claim 2 recites a block of OR gates, but it does not specify whether they are in or out of the cells. No location is specified for the single OR gate of Claim 8. Claim 10 references a feedback connection from the OR gates. These claims include within their scope devices that have OR gates either inside or outside of the cell.

97. As noted earlier, claim 3 is inconsistent with the description (pages 9, 13, Figures 3-4) in that it provides for the transferring of the function word directly to the output terminals. So even from the claims, the location of the OR gates is not clear.

98. As for their connectivity, looking to Figure 12 of Dancea[1], the "OR ports" block is shown to traverse the right boundary of the illustrated basic cell, just like the input terminals. Thus, it is clear that the OR ports extend to each of the basic cells. This begs comparison to the "AND ports" block which, correctly, stays within the confines of the basic cell. Again, the details of how the OR gates are wired and how many OR gates are present

in the block, is not explicitly shown in Figure 12. However, again, the skilled reader is credited with an understanding of the product terms method which guides them when putting the VLSI circuit shown in Figure 12 into practice. With the connectivity of the OR gates being clear to the skilled reader, whether they are located inside or outside of the basic cells would provide the same result. Therefore, even though the claims are silent as to the location of the OR gates, the Board concludes that the location of the OR gate or gates is not a feature which materially affects the way the alleged invention works.

99. Regarding the exact number of OR gates as compared to Dancea[1], the Board references our analysis of claim 2 in which the Board concluded that the number of OR gates is determined when implementing the product terms method in both Dancea[1] and the instant application. The Board is unable to validate the proposition that the location of the OR gates impacts the number of the OR gates required in the VLSI device.

Control Block

100. The Applicant points to the provision of a Acontrol block@ in the Dancea[1] VLSI example in Figure 12 as a difference compared to the subject matter of the present claims. In the Applicant=s letter of January 21, 2002, he states on page 5:

> A...[discussing control signals on the AND and OR gates] and the applicant added in the schema of Figure 12 (publication Dancea1) the Acontrol@ the Acontrol block@. This block had the role to send the control signals through ports to validate the flow of information.
>
> ...
>
> Consequently, the patent application eliminates also the control block.@

101. In his letter of October 21, 2002, the Applicant states at page 3:

> AWhen the control signals exist, the biggest part of the control block is dedicated to manage these control signals. Evidently, a control block must exist for all types of logical VLSI circuits, because this control block has other tasks, like to load registers, to create address paths, to clear information in registers, to change the state of a cell from active to passive and vice versa, and so on.@

102. First, whether or not a control block is present in Figure 12 is a moot point with respect to anticipation. A claim is anticipated whenever a prior disclosure gives enough information to inevitably lead the skilled reader to the subject matter claimed. Whether or not further elements are present in the prior disclosure is of no concern unless explicitly excluded from the claimed subject matter. Thus, the findings in view of Dancea[1] are not affected by inclusion or exclusion of the control block.

103. Figure 12 of Dancea[1] indeed shows a control block. In describing the control block, page 50 of the article states:

> AThe control part allows us to load the register of the cells and consequently to change dynamically the logical behaviour of the structure.@

104. There is a contradiction in the Applicant=s submissions quoted above. In his letter dated January 21, 2002, he states, in an attempt to distinguish over Dancea[1], that the present application eliminates the need for a control block. On the other hand, the Applicant (who is the author of Dancea[1]) in his letter dated October 21, 2002, acknowledges that a control block must exist to load registers, create address paths, and so on.

105. Further, the description of the instant application does not state how, *inter alia*, the various registers of the device are controlled. It is left to the skilled reader to supplement the teachings of the Applicant with their skill and knowledge in the art of digital design. As the Applicant himself points out, a control block is required for all types of VLSI circuits. The Applicant=s implementation does not avoid the requirement to provide means to address and control data transfer to storage elements, including the memory word registers, within the VLSI device.

106. The Board concludes that the present claims do not patentably differ from the Dancea[1] article with regard to the control block feature.

Method of Synthesis

107. The Applicant states that the VLSI devices of the present application could not have been developed using "classical synthesis", but rather that "perfect induction" was used instead in its development. This argument does not bear any relevance to the rejection as it overlooks the disclosure of a VLSI circuit in the Dancea[1] article. Thus, the person skilled in the art has the VLSI circuit as their start point. The development of the layout of the VLSI implementation had been done for them and made available to the public. As such, the Board need not consider what manner of development the Applicant used and whether other modes would not give the claimed subject matter.

Summary of findings: Anticipation

108. Therefore, the Board finds that the use of ports vs gates, location and number of OR

gates, absence of a control block, and method of synthesis, are not factors which disturb our findings. The Board concludes that claims 1 to 12 are anticipated in view of Dancea[1].

OBVIOUSNESS

109. In the Final Action, the Examiner alleged that claims 1 to 12 were obvious under Section 28.3 of the *Patent Act*, in view of Dancea[1], Dancea[2] and cited an additional reference, Dancea[3]. Claims 1 to 12 are anticipated by Dancea[1]. Therefore, the Board considers that there can be no inventive step over the prior art in claims 1 to 12.

110. With reference to claim 2, assuming arguendo that the input register was an essential element, the Board finds that the difference of including an input register does not impart inventive ingenuity to the claim.

111. To begin with, the Applicant has not made any submission to either the Examiner or the Board to the effect that the difference, if there is one, over Dancea[1] of providing an input register renders the claim inventive.

112. The use of a register to store input (or other) variables for use in a combinational circuit is commonplace in electrical engineering. They are known to be used, for example, in conjunction with the I/O (input/output) interface of peripherals. This is taught in undergraduate logic design and computer architecture courses and is common general knowledge. Were the argument made to the contrary, evidence showing that it was common general knowledge could be found in introductory texts on logic design or computer architecture.

113. While Dancea[1] does not explicitly teach the use of an input register, the Board is of the opinion that it was not discussed therein as it was immaterial to the operation of the invention. So long as input terminals were provided, as they are in Dancea[1], the VLSI circuit would have worked in the same way as described in the present application. One of ordinary skill in the art would, as of the claim date, have been directly led to the inclusion of an input register in the VLSI device taught in Dancea[1].

INOPERATIVENESS: SECTION 2

The Examiner=s position

114. In the Final Action, the Examiner rejected claim 12 for inoperativeness, stating [emphasis added]:

> Inoperativeness
>
> Claim 12 recites the elements of an expert system, including several "means for inputting;" but, as claimed, the nature of said inputting means is unclear. It is not clear if the expert system inputs the variables or equations into some other structure, or if the expert system receives inputs from an external agent or device.
>
> Claim 12 is directed toward the various elements which comprise the expert system, and as such, it is unclear how the method step of "loading said behavioural list . . ." relates to the means recited by the claims. A claim to a method must be defined by the steps comprising the method rather than system structure.

Claim 12 thereby does not comply with section 2 of the Patent Act for lack of utility because the claim is incomplete and fails to recite sufficient elements for proper practice of the claimed invention

115. The Board has reviewed the Examiner=s objection to claim 12 under Section 2 of the *Patent Act*. The reason provided by the Examiner in the first paragraph is concerned with the clarity of the claimed Ameans for inputting@, rather than inoperativeness.

With respect to the second paragraph of the Examiner=s inoperativeness objection, it appears to be directed to the recitation in a method claim of a structure rather than steps. Generally, the Board sees no difficulty with reciting a structure that further defines a system used in a method claim.

116. However, the Board has noted the Examiner=s concern about the relation between the step of Aloading said behavioural list@ and the preceding Ameans for@ statements. The structure in claim 12 is defined as Asaid expert system program . . . comprises . . . means for . . .@ In the sense used in this application, and as widely accepted in this field, a program is a set of computer executable instructions that are grouped together to accomplish a task or tasks. Often, the sequence in which these instructions are carried out, is critical. Therefore, programs are conventionally claimed as steps in a method claim. The sequential execution, if any, of the Ameans forA components of the expert system program, may be important. Thus, it can=t be presumed, for example, that the step of loading said behavioural list has any particular sequential relation with the preceding Ameans for@ structures. The Final Action does not establish whether it is this sequential Arelation@ that forms the basis of the Examiner=s objection. Therefore,

other than noting our concern, the Board is unable to make a determination on this ground.

117. The third paragraph seems to point to a lack of sufficient elements in claim 12. Claim 1 is properly defined using steps, and was not found to be inoperable by the Examiner. Since claim 12 depends on claim 1, the Board cannot sustain the objection that claim 12 contains insufficient elements for proper operation of the invention.

118. Based on the Examiner=s arguments, the Board recommends the Examiner=s objection under Section 2 of the Patent Act be reversed.

Recommendation

119. The Board has noted numerous irregularities in the claims. For example, claim 8 is dependant on claim 1, but does not provide proper antecedent basis for the expressions Asaid n cells@ and Asaid product terms@. Similar comments apply to Asaid OR gates@ and Asaid input register@ in claim 10. The terminology in the claims is also confusing, and sometimes contradictory. In claim 1, for example, it is not clear what are the inputs to the r OR gates and r output terminals, and whether the input variables alone are used for determining the logical value of the product term. Claim 11 confusingly references different features from both claims 1 and 3.

120. In summary, the Board recommends that:

1. The Examiner=s objection to claims 1 to 12 under Section 28.2(1)(a) of the *Patent*

Act, for being anticipated by Dancea[1], be affirmed;

2. The Examiner=s objection to claims 1 to 12 for being obvious under Section 28.3 of the *Patent Act*, be affirmed;

3. The Examiner=s objection to claim 12 under Section 2 of the *Patent Act*, be reversed; and,

4. The rejection of the application be affirmed.

M. Gillen

Member

121. I concur with the findings and the recommendation of the Patent Appeal Board. Accordingly, I refuse to grant a patent on this application. Under Section 41 of the *Patent Act*, the Applicant has six months within which to appeal my decision to the Federal Court of Canada.

Mary Carman

Commissioner of Patents

Dated at Gatineau, Quebec,

this 30 day of April , 2008