COMMISSIONER'S DECISION

Sec. 2: TOLL COMMUNICATIONS SWITCHING SYSTEM

A switching system wherein the common memory is accessible from a first and a second processor for storing data representing conditions of the peripheral circuits being completed is patentable under Section 2.

Final Action: Reversed.

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Patent application 164,446 (Class 354-233), was filed on Feb. 23, 1973 for an invention entitled DATA PROCESSING FOR A TOLL COMMUNICATIONS SWITCHING SYSTEM. The inventors are Juliaan L.G. Janssens et al. The Examiner in charge of the application took a Final Action on June 23, 1978 refusing to allow it to proceed to patent.

The subject matter of this application relates to a telecommunications switching network being controlled by computer processors via peripheral interfacing circuits. Each processor includes self contained memory for storing computer programs, and each has access to a further common memory for storing data representing conditions of the peripheral interfacing circuits. Figure 1 of the application is shown below.

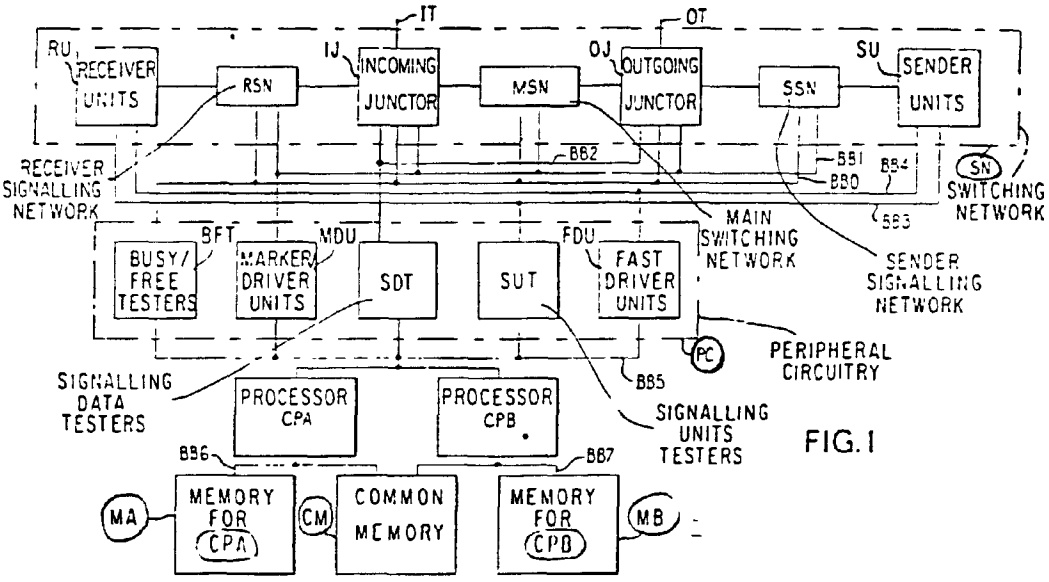

FIG. 1

The switching system includes the switching network SN, the peripheral circuitry PC, two processors CPA, CPB, a common memory CM and individual memories MA and MB.

In the Final Action the Examiner rejected the claims as defining unpatentable subject matter under Section 2 of the Patent Act. That action stated (in part):

> Applicant's alleged invention relates to a data processing system including a plurality of processors and a controllable arrangement of telecommunications switching equipment. The processors control the arrangement through execution of a plurality of programs. The disclosure includes pertinent flow charts in the drawings in support of the computer programs.
>
> Applicant argues that the "claims as now presented are directed to an automatic communications switching system comprising a switching network, a data processing network and a plurality of peripheral circuits". Further, applicant argues that "the claims now presented are drawn to statutory subject matter".
>
> On February 28, 1978 the PAB issued a set of guidelines which included:
>
> 1. Claims to a program per se are not patentable;
> 2. Claims to a new method of operating a computer are not patentable;
> 3. Claims to a computer programmed in a novel manner, expressed in any and all modes, where the novelty lies solely in the program or algorithm, are not directed to patentable subject matter under Section 2 of the Patent Act.
> 4. Claims to a computing apparatus programmed in a novel manner, where the patentable advance is in the apparatus itself, are patentable.
>
> Applicant's claims are still directed to a plurality of processors which control the completion and supervision of calls through the switching system by the execution of programs. The novelty lies in the execution of programs. There is no new apparatus claimed.

In response to the Final Action the Applicant stated (in part):

> Previously, the Examiner had cited the four guidelines issued by the Patent Appeals Board on February 28, 1978. No application of the claims to the specific guidelines was made.

> Viewing the guidelines, clearly the claims are not directed to a program per se. Thus, guidelines #1 is not applicable. The claims are not drawn to a new method of operating a computer. Thus, guideline #2 is inapplicable. Guideline #3 calls for a computer programmed in a novel manner expressed in any and all modes. Applicant does not claim a computer programmed in a novel manner. Thus, guideline #3 is inapplicable.
>
> Guideline #4 states that claims to a computing apparatus programmed in a novel manner where the patentable advance is in the apparatus itself are patentable. While this guideline is not directly applicable, it may be closer than the others.
>
> The present application is more closely directed to what has been called "Consumer Application Programming" in which a computer is connected into a system to perform a system function. However, the present invention is directed to an arrangement for tying together a plurality of computers in real time to process random incoming calls and to allocate the calls between the computers based on the imposition of separate memories to store data controlling the interaction of the plural computers.

The issue before the Board is whether or not the claims are directed to patentable subject matter in view of Section 2 of the Patent Act. Claim 1 reads:

> An automatic communications switching system comprising a switching network for completing calls through the system, a data processing network for controlling the completion and supervision of calls through the system by the execution of programs, and a plurality of peripheral circuits interfacing between said switching network and data processing network to provide signals regarding the condition of the switching network to the processing network and for transmitting signals from the processing network for controlling and supervising the operation of the switching network, and in which said data processing network includes a first and a second processor, a first individual memory normally accessible only to the first processor for storing data including programs of a first

> set concerning calls being handled by said first processor, a second individual memory normally accessible only to the second processor for storing data including programs of said first set concerning calls being handled by said second processor, means in individual memories for storing address information of calls through peripheral circuits, the calls being handled by the processor associated with the respective individual memory, a further memory commonly accessible from both said first and said second processor for storing data representing conditions of said peripheral circuits being completed through said peripheral circuits under the control of both said processors in a load sharing manner and, in which each of said processors includes means to prevent said programs of said second set from being simultaneously executed by both processors to thereby give rise to conflicting situations due to the simultaneous handling of similar programs, said preventing means comprising a storage table individual to each processor, said table indicating the programs to be handled and not to be handled by the particular processor.

It is the Examiner's position that the alleged invention relates to a data processing system in which the processors control the arrangement through execution of a plurality of programs wherein the novelty lies in the execution of these programs. On the other hand the Applicant argues that this invention is directed to a "plurality of computers in real time to process random incoming calls" and to allocate these calls between the computers utilizing their individual separate memories and a memory common to all computers for storing data to control the interaction of the computers.

In considering the issue as developed by the Examiner and as argued by the Applicant, we are guided by the Federal Court decision in Schlumberger Canada Ltd. v The Commissioner of Patents 56 CPR (2d) at 204 (1981). Being handed down in 1981, the decision was not, of course, available to assist either the Examiner or the Applicant when the Final Action was taken. In that decision involving computer-related subject matter, Pratte J. has these comments:

> In order to determine whether the application disclosed a patentable invention, it is first necessary to determine what, according to the application, has been discovered.

and

> I am of opinion that the fact that a computer is or should be used to implement discovery does not change the nature of that discovery

From the disclosure we are informed that a data processing system is found in U.S. patent 3,557,315 to S. Kobus et al wherein each of the processors is able to execute all of the programs needed to control all the operations required to establish a call communication through the switching equipment. To prevent a processor from executing simultaneously with another processor which could lead to conflicting situations, inhibiting means are required by Kobus.

This application does not require inhibiting means as it divides the programs into a first series which are executed by one processor, and into a second series wherein the execution is by at least two processors. By allocating the series in this manner it regulates access to the processors thereby eliminating the need of queuing the series for processing, as required by prior art systems.

Another characteristic described in this application is that the processors are interconnected by interprocessor communication means to transfer information between the processors by the use of a common memory means.

Common memory means are known as described in the disclosure by reference to U.S. patent 3,503,048 which also relates to telecommunication switching equipment utilizing a common memory. This patent describes a system of establishing call communications by executing a plurality of programmes and each of these programmes is carried out by one predetermined processor. That system provides extensive distribution of programmes among all the processors which requires them to operate in succession for each call to be established. As the transfer of information between processors is made through common memory and as none of the programmes is executed by two or more processors, a waiting time is involved due to the queuing of the programmes as they await processing, thereby increasing the length of time to complete a call.

As stated in this application, the improvement lies in an orderly redistribution of programmes between the processors. The Applicants' data processing system distributes the programmes selectively among the processors by allocation, according to coded mask words, so that some programmes are distributed to a plurality of processors and others are handled by one processor only. The application states that such flexibility is useful "when there is one long programme which cannot be readily matched as far as time of execution is concerned by a plurality of shorter programmes".

Figure 5 (shown below) schematically illustrates components of the Applicant's common memory including memory tables and mask controls.

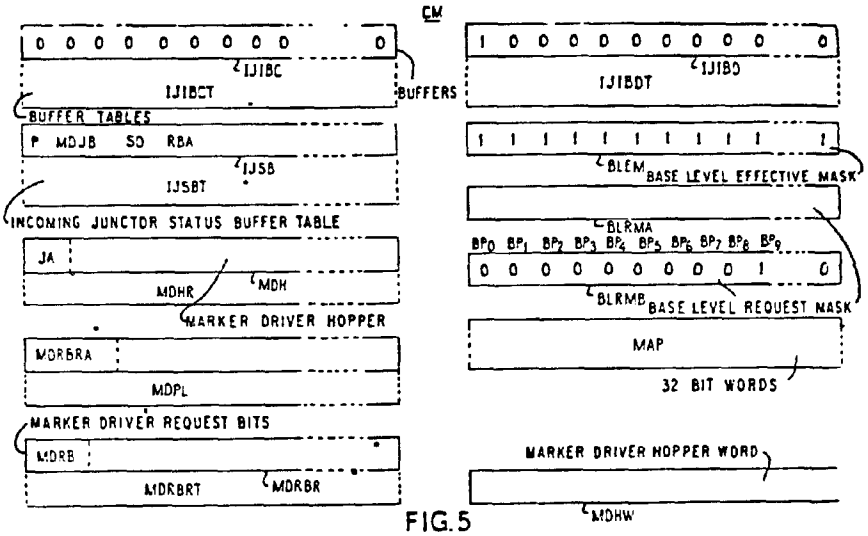

FIG.5
MEMORY CM

The masking arrangement shown uses reference data in terms of 32-bit words to store the busy/free conditions of the elements of the system, such as the incoming and outgoing junctors, the main switching network and the signal sending network. The incoming junctor status buffer table (IJSBT) stores all information relating to call communications involving this junctor. A marker driver hopper table forms a waiting list of information to be handled by the marker driver unit. The base level effective mask (BLEM) indicates base level programs which must not be executed due to the unavailability of information. Since the BLEM is stored in the common memory it is valid for both processors, and both processors

are able to modify it. Base level request masks (BLRMA) (BLRMB) indicate the base level programs which must be executed as soon as possible by processor CPA or CPB respectively and independently from other conditions.

Claim 1 is directed to an automatic communications switching system wherein a common memory is accessible from a first and a second processor for storing data representing conditions of the peripheral circuits being completed. These peripheral circuits are defined in the claim as being under the processors in a load sharing manner wherein each processor includes means to indicate the programs it is or is not able to handle, thereby speeding up the processing. We are satisfied that this claim and claims 2 to 4 define more than algorithms or calculations and are more than the mere execution of programs. We find they are properly directed to the Applicant's discovery.

In summary we recommend that refusal of the claims be withdrawn and the application be returned to the Examiner.

A. McDonough
Chairman
Patent Appeal Board

M.G. Brown
Assistant Chairman

S.D. Kot
Member

I concur in the findings and the recommendation of the Patent Appeal Board. Accordingly, I withdraw the Final Action and remand the application to the Examiner.

J.H.A. Gariépy
Commissioner of Patents

Dated at Hull, Quebec

this 15th. day of August, 1984

Agent for Applicant

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